

**EAST - [10707826.wsp:1]**

File View Edit Tools Window Help

Search

DEs:  US-PG-PUB:USPAT,EPO,JPC ☐ Flash

Default operator:  OR ☒ Highlight all hit terms initially

1 and (floating near gate with concave) and control near gate

☐ Drafts  
☐ Pending  
☒ Active  
☐ Failed  
☐ Saved  
☐ Favorites  
☐ Tagged (0)  
☐ UDC  
☐ Queue  
☐ Trash

☐ L1: (101086) (flash near memory or non-volatile near memory)  
☐ L2: (22822) floating near gate\$1  
☐ L3: (11968) 1 and 2  
☐ L4: (163) 3 and concave  
☐ L5: (2586) 3 and stack\$2 near gate  
☐ L6: (2379) 5 and (oxide dielectric)  
☐ L8: (1) 7 and concave  
☐ L7: (63) 6 and (erase near gate) and (select near gate)  
☐ L9: (19146) 1 and (NAND NOR)  
☐ L10: (16) 9 and (floating near gate with concave)  
☐ L11: (49) 1 and (floating near gate with concave) and control near gate  
☐ L12: (8927) 1 and (floating near gate) and control near gate  
☐ L13: (39) 1 and (floating near gate) and control near gate and erase near gate and select near gate

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
33	<input type="checkbox"/>	<input type="checkbox"/>	US 6482700 B2	20021119	10	Split gate field effect transistor (FET) device with enhanced electrode registration and method for fabrication thereof	438/267	257/E21.682; 257/E27.103; 257/F79.179
34	<input type="checkbox"/>	<input type="checkbox"/>	US 6469341 B1	20021022	14	Method and device for producing undercut gate for flash memory	257/316	257/E21.209; 257/E27.103; 257/F79.179
35	<input type="checkbox"/>	<input type="checkbox"/>	US 6468663 B2	20021022	9	Split gate field effect transistor (FET) device employing dielectric barrier layer and method for fabrication thereof	438/261	257/E21.682; 257/E27.103; 257/F79.179
36	<input type="checkbox"/>	<input type="checkbox"/>	US 6387757 B1	20020514	8	Sacrificial self aligned spacer layer on implant mask method for forming a split gate field effect transistor (FET) device	438/266	257/E21.682; 257/E27.103
37	<input type="checkbox"/>	<input type="checkbox"/>	US 6372617 B1	20020416	12	Method of manufacturing non-volatile memory	438/593	257/E21.209; 257/E21.422; 438/594
38	<input type="checkbox"/>	<input type="checkbox"/>	US 6355525 B1	20020312	16	Method of producing non-volatile semiconductor memory device having a floating gate with nonuniform conductive side-wall notches	438/257	257/E21.209; 257/E21.422; 257/F79.179
39	<input type="checkbox"/>	<input type="checkbox"/>	US 6317360 B1	20011113	54	Flash memory and methods of writing and erasing the same as well as a method of forming the same	365/185.01	257/315; 257/E21.209; 257/F71.477; 257/E21.682; 257/E27.103; 438/754
40	<input type="checkbox"/>	<input type="checkbox"/>	US 6248631 B1	20010619	15	Method for forming a v-shaped floating gate	438/260	257/E21.209; 257/E21.688; 438/757
41	<input type="checkbox"/>	<input type="checkbox"/>	US 6245613 B1	20010612	12	Field effect transistor having a floating gate	438/259	257/E21.209; 257/E21.688; 438/757
42	<input type="checkbox"/>	<input type="checkbox"/>	US 6204122 B1	20010320	18	Methods of forming nonvolatile integrated circuit memory devices having high capacitive coupling ratios	438/257	257/E21.209; 257/E21.682; 257/F79.179
43	<input type="checkbox"/>	<input type="checkbox"/>	US 6172394 B1	20010109	16	Non-volatile semiconductor memory device having a floating gate with protruding conductive side-wall notches	257/315	257/288; 257/387; 257/F71.209